

CLAIMS

What is claimed is:

- 5 1. A method of modeling a light emitting diode device comprising:
 automatically generating a netlist from a computer-aided design layout;
 and
 executing the netlist to produce an output correlative to current spreading
 uniformity for the light emitting diode device.
- 10 2. The method, as set forth in claim 1, wherein automatically generating a
 netlist comprises automatically generating a netlist having at least 60,000 lines.
- 15 3. The method, as set forth in claim 1, comprising producing a plurality of
 contour plots correlative to the current spreading uniformity for the light emitting diode
 device.
- 20 4. The method, as set forth in claim 1, comprising producing an output
 correlative to thermal performance of the light emitting diode device.
- 25 5. The method, as set forth in claim 1, comprising producing an output
 correlative to optical performance of the light emitting diode device.
- 30 6. A method of modeling a light emitting diode device comprising:
 generating a computer-aided design layout of the light emitting diode
 device;
 fracturing the layout to convert design geometries into orthogonal
 rectangles defined by coordinates;
 scaling the layout to a specified element size, wherein the scaled layout
 includes each of a plurality of nodes, a plurality of resistors and a

plurality of diodes each having a layer number and a unique coordinate associated therewith;
automatically generating a netlist from the scaled layout; and
executing the netlist to produce an output correlative to current
5 spreading uniformity for the light emitting diode device.

7. The method, as set forth in claim 6, comprising producing a plurality of contour plots correlative to the current spreading uniformity for the light emitting diode device.

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8. The method, as set forth in claim 6, comprising producing a tabular output correlative to the current spreading uniformity for the light emitting diode device.

9. The method, as set forth in claim 6, comprising naming each of the nodes such that a name of each node includes the layer number and the unique coordinate associated therewith.

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10. The method, as set forth in claim 6, comprising naming each of the elements such that a name of each element includes an element type, the layer number and the unique coordinate associated therewith.

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11. The method, as set forth in claim 6, comprising before executing the netlist, manually supplementing the netlist with information correlative two power connections.

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12. The method, as set forth in claim 6, comprising before executing the netlist, manually supplementing the netlist with information correlative to elements oriented in the vertical direction of the light emitting diode device.

13. The method, as set forth in claim 6, comprising before generating the netlist, automatically eliminating any of the plurality of nodes having less than two of the plurality of resistors coupled thereto.

5 14. A method of modeling a light emitting diode device comprising:
fracturing a computer aided design layout corresponding to the light
emitting diode device to convert design geometries into
orthogonal rectangles defined by coordinates;
scaling the layout to a specified element size;
10 adding a corresponding layer number and element value to elements and
nodes in each of the orthogonal rectangles;
automatically generating a netlist from the scaled layout;
executing the netlist to produce a simulation output file;
calculating currents associated with each of the elements; and
15 producing a current output file comprising the currents associated with
each of the elements.

15 15. The method, as set forth in claim 14, comprising converting the
simulation output file into tabular form.

20 16. The method, as set forth in claim 14, comprising producing a plurality of
contour plots from the current output file, wherein the contour plots are correlative to the
current spreading uniformity of the light emitting diode device.

25 17. The method, as set forth in claim 14, comprising naming each of the
elements such that a name of each element includes an element type, the layer number
and the unique coordinate associated therewith.

18. The method, as set forth in claim 14, comprising naming each of the nodes such that a name of each node includes the layer number and the unique coordinate associated therewith.

5 19. The method, as set forth in claim 14, comprising before generating the netlist, automatically eliminating any of the nodes having less than two of the elements coupled thereto.

20. A method of modeling a light emitting diode device comprising:
10 automatically generating a netlist from a computer-aided design layout of the light emitting diode device, wherein the design layout comprises each of a plurality of nodes, a plurality of resistors and a plurality of diodes;
 uniquely naming each of the plurality of nodes, the plurality of resistors
15 and the plurality of diodes in accordance with location within the design layout to produce a unique name corresponding therewith;
 and
 modeling the light emitting diode device using the netlist to produce a modeling output, wherein the modeling output comprises the
20 unique name corresponding to each of the plurality of nodes, the plurality of resistors and the plurality of diodes.

21. The method, as set forth in claim 20, wherein uniquely naming each of the plurality of resistors and each of the diodes comprises producing a unique name
25 corresponding therewith and comprising an element type, a layer number and a unique coordinate associated therewith.

22. The method, as set forth in claim 20, wherein uniquely naming each of the plurality of nodes comprises producing a unique name corresponding therewith and
30 comprising a layer number and the unique coordinate associated therewith.

23. A computer-readable medium storing computer instructions for:
automatically generating a netlist from a computer-aided design layout
corresponding to a light emitting diode device.
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24. A computer-readable medium storing computer instructions for:
fracturing a computer-aided design layout corresponding to a light
emitting diode device to convert design geometries into
orthogonal rectangles defined by coordinates;
10 scaling the layout to a specified element size, wherein the scaled layout
includes each of a plurality of nodes, a plurality of resistors and a
plurality of diodes each having a layer number and a unique
coordinate associated therewith; and
automatically generating a netlist from the scaled layout.
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25. The computer-readable medium, as set forth in claim 24, comprising
computer instructions for before generating the netlist, automatically eliminating any of
the plurality of nodes having less than two of the plurality of resistors coupled thereto.
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26. The computer-readable medium, as set forth in claim 24, comprising
computer instructions for producing a plurality of contour plots correlative to the current
spreading uniformity for the light emitting diode device.
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27. The computer-readable medium, as set forth in claim 24, comprising
computer instructions for producing a tabular output correlative to the current spreading
uniformity for the light emitting diode device.
28. A computer-readable medium storing computer instructions for:

fracturing a computer aided design layout corresponding to a light
emitting diode device to convert design geometries into
orthogonal rectangles defined by coordinates;
scaling the layout to a specified element size;
5 adding a corresponding layer number and element value to elements and
nodes in each of the orthogonal rectangles;
automatically generating a netlist from the scaled layout; and
producing a contour plot corresponding to current uniformity in the
light emitting diode device and correlative to an executed
10 simulation of the netlist.